

Fig.1 (Prior Art)

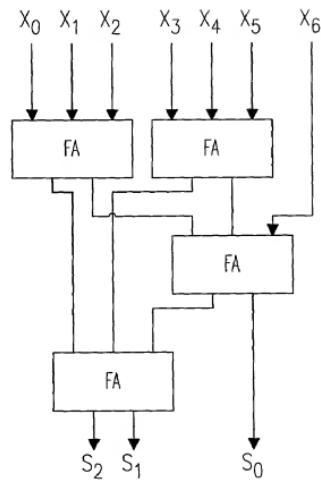


Fig.2 (Prior Art)

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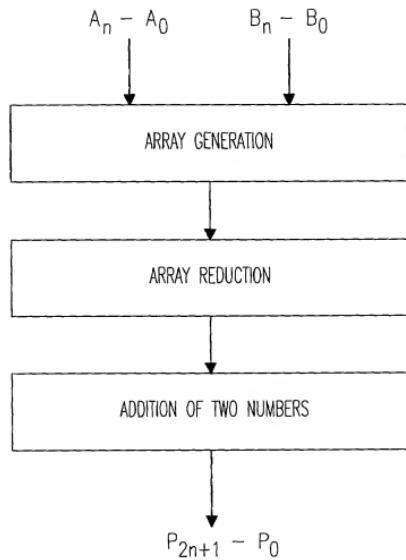


Fig.3 (Prior Art)

A₇B₀ A₆B₀ A₅B₀ A₄B₀ A₃B₀ A₂B₀ A₁B₀ A₀B₀
A₇B₁ A₆B₁ A₅B₁ A₄B₁ A₃B₁ A₂B₁ A₁B₁ A₀B₁
A₇B₂ A₆B₂ A₅B₂ A₄B₂ A₃B₂ A₂B₂ A₁B₂ A₀B₂
A₇B₃ A₆B₃ A₅B₃ A₄B₃ A₃B₃ A₂B₃ A₁B₃ A₀B₃
A₇B₄ A₆B₄ A₅B₄ A₄B₄ A₃B₄ A₂B₄ A₁B₄ A₀B₄
A₇B₅ A₆B₅ A₅B₅ A₄B₅ A₃B₅ A₂B₅ A₁B₅ A₀B₅
A₇B₆ A₆B₆ A₅B₆ A₄B₆ A₃B₆ A₂B₆ A₁B₆ A₀B₆
A₇B₇ A₆B₇ A₅B₇ A₄B₇ A₃B₇ A₂B₇ A₁B₇ A₀B₇

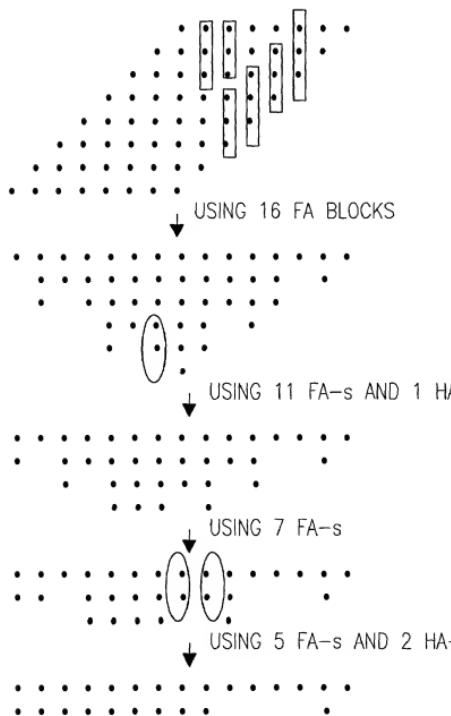


Fig.4 (Prior Art)

TITLE: MULTIPLICATION LOGIC CIRCUIT
INVENTORS NAME: Sunil Talwar et al.
DOCKET NO.: 1365.048US1

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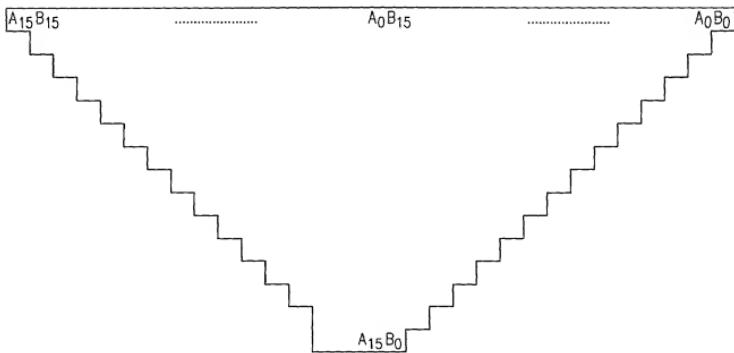


Fig.5

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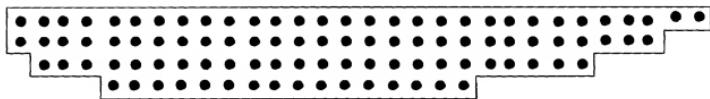


Fig.6

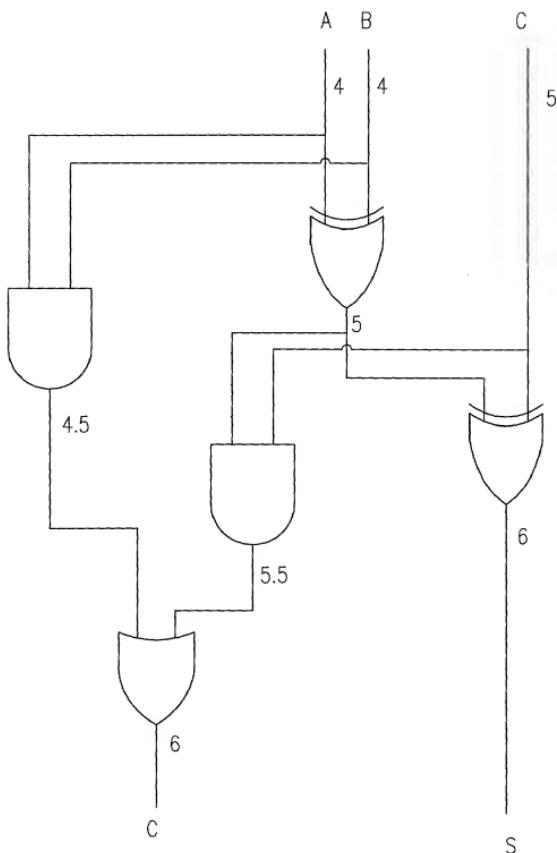


Fig. 7

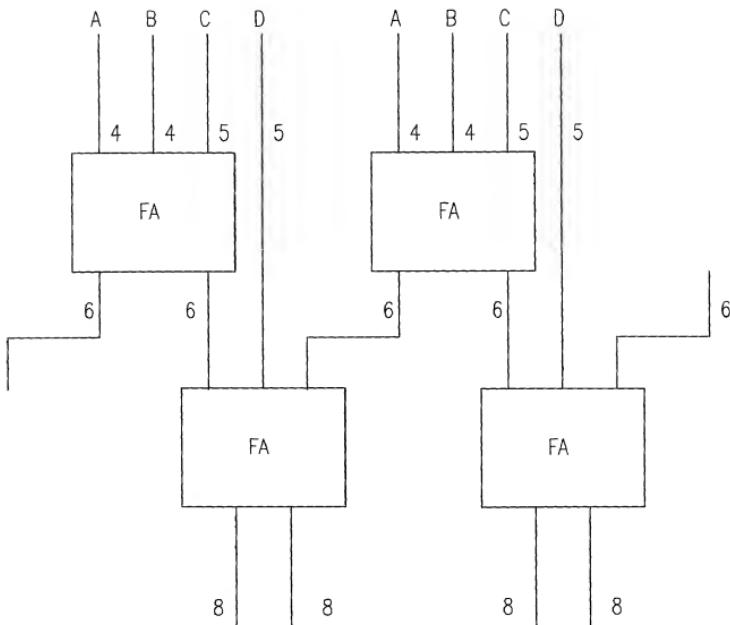


Fig. 8

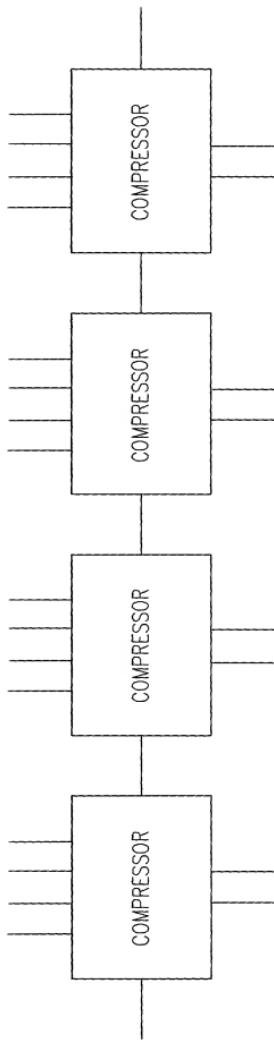


Fig. 9

TITLE: MULTIPLICATION LOGIC CIRCUIT
INVENTORS NAME: Sunil Tolwari et al.
DOCKET NO.: 1365.048US1

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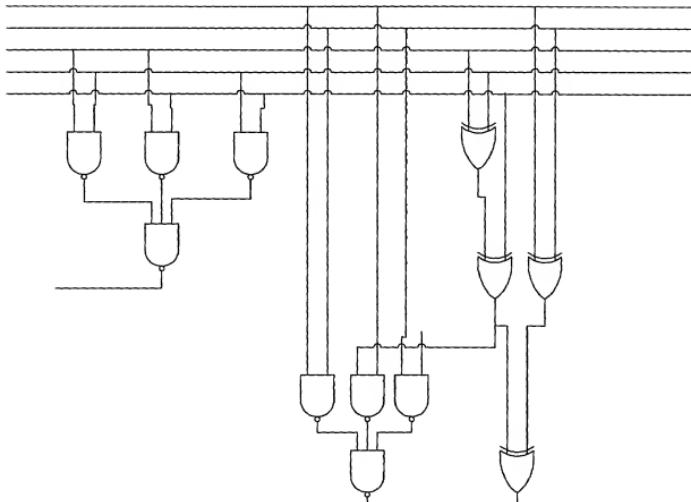


Fig. 10